QLx411G Evaluation Board User Guide

Introduction to QLX411G Evaluation Kit

The QLX 411G series Evaluation Board is a versatile stand-alone card developed to evaluate the performance of Intersil QLx411G series Quad Equalizer.

The evaluation kit includes:

- QLX411G evaluation board
- Power cable

The key features of the evaluation board are:

- QLX411G series IC
- Single 5V external power supply
- On board DC/DC converter that provides 1.2V supply to the IC
- 8 sets of SMA connectors for high speed signals input and output
- 4 sets of 50Ω terminators on the channel outputs
- A variable potentiometer to set DT
- Boost setting for each channel via two sets of headers

Operation of the QLX411G Evaluation Board

After a brief description of the board design and layout we will describe the different features and options to operate the board. In particular we will describe:

- The power supply to the board
- The high speed differential I/Os
- The variable Detection Threshold
- The Control Boost setting

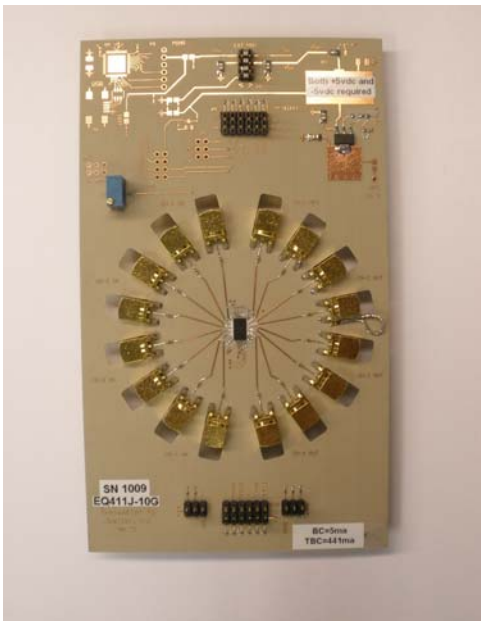

FIGURE 1. QLx411G EVALUATION BOARD EXTERNAL POWER SUPPLY CONNECTOR

Power Supply

The Evaluation Board requires an independent external 5.0V power supply. On board voltage regulators supply the appropriate 1.2V to the QLx411G IC.

Power is supplied to the board via header P1 highlighted on Figure 2. P1 connectivity is specified in Table 1. The typical current consumption for the board including the voltage regulator and the IC is 440mA with all channels active.

POWER SUPPLY CONNECTOR

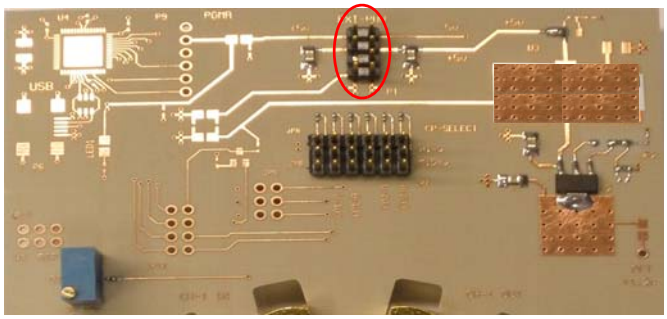

FIGURE 2. QLx411G EVALUATION BOARD EXTERNAL POWER SUPPLY CONNECTOR

TABLE 1. DESCRIPTION OF CONNECTOR P1

8 – NC	7 – NC
6 – 5.0V	5 – 5.0V
4 – NC	3 – NC
2 – GND	1 – GND

High Speed Data I/O Interface Connectors

There are sixteen SMA connectors on the board, eight for the CML differential inputs and eight for the CML differential outputs. All the connections from the SMA connectors to the QLX411G chip are AC coupled with a 220nF broad band capacitor.

During operation all unused channel I/Os need to be properly terminated with 50Ω terminators.

Detection Threshold (DT)

The QLx411G contains special lane management capabilities to detect and preserve periods of line silence while still providing the fidelity-enhancing benefits of limiting amplification during active data transmission. Line silence is detected by measuring the amplitude of the equalized signal and comparing that to a threshold set by the voltage at the DT pin. When the amplitude falls below the threshold, the output driver stages are muted and held at their nominal common mode voltage.

The DT voltage can be changed on the QLx411G evaluation board by adjusting the potentiometer VR1 (Figure 3). Typically the potentiometer should be set so that the voltage between the adjacent 0Ω resistor and ground is 500mV.

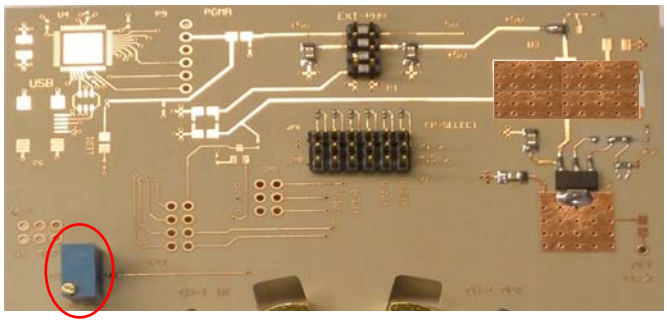

FIGURE 3. QLx411G EVALUATION BOARD DT POTENTIOMETER

Loss of Signal (LOS) indicator

QLx411G LOS[k] pins are used to output the state of the muting circuitry to serve as a loss of signal indicator for channel k. This signal is directly derived from the muting signal off the DT-threshold signal detector output. The LOS signal goes 'HIGH' when the power signal is below the DT threshold and 'LOW' when the power goes above the DT threshold. This feature is meant to be used in optical systems (e.g. QSFP) where there are no quiescent or electrical-idle states. In these cases, the DT threshold is used to determine the sensitivity of the LOS indicator.

On the QLx411G evaluation board the LOS[k] pins are accessible through two 3x2 headers, JP4 and JP5 (Figure 4). A voltage reading superior to 1V shall be interpreted as Loss of Signal, whereas a reading inferior to 250mV shall be interpreted as a valid signal.

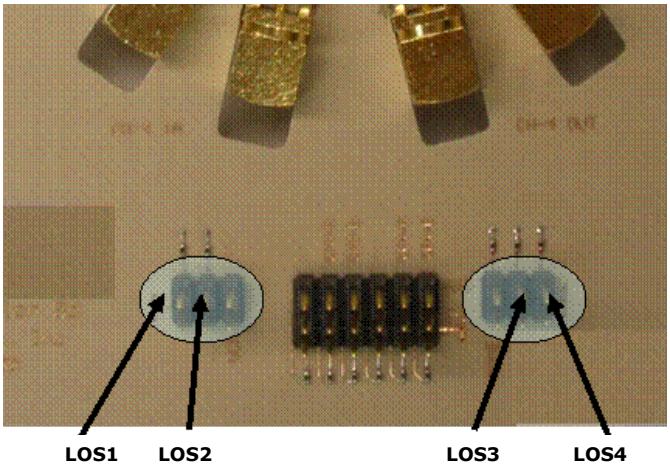

FIGURE 4. LOS INDICATORS ON QLx411G EVALUATION BOARD

TABLE 2. JP4 AND JP5 CONNECTIVITY

JP4		
2- LOS1	4- LOSS2	6- GND
1- GND	3- GND	5- GND

JP5		
2- Mode	4- LOS4	6- LOS3
1- GND	3- GND	5- GND

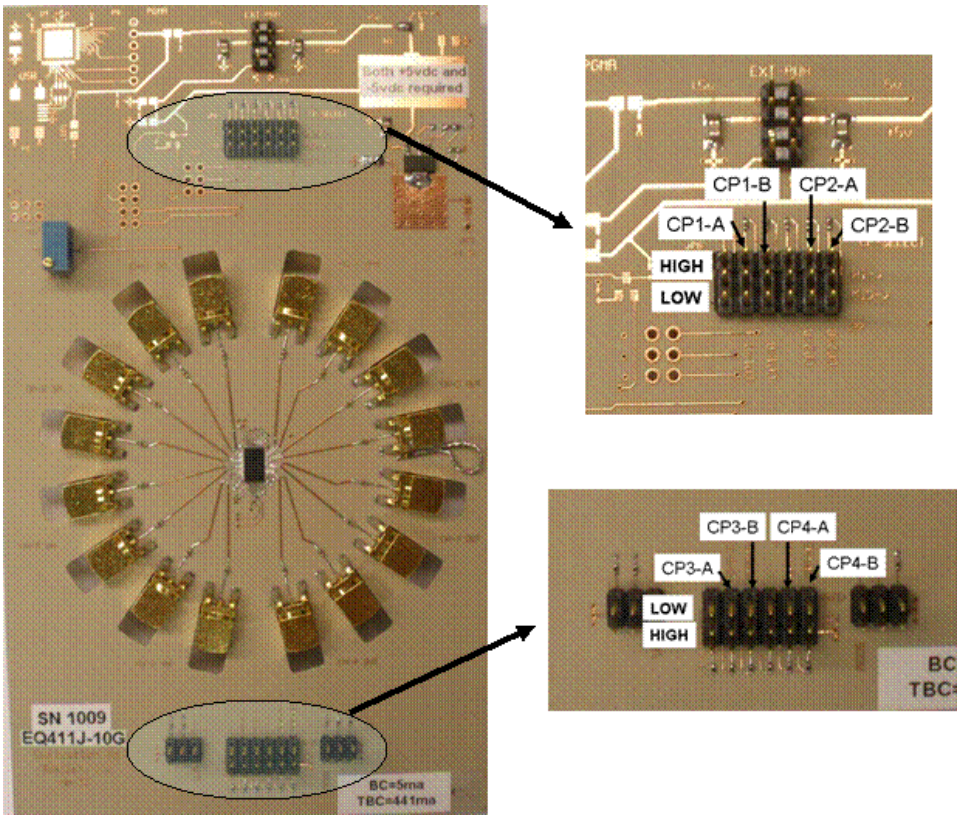

FIGURE 5. EQUALIZER BOOST CONTROL HEADERS

Boost Setting Control

The boost setting configuration (compensation setting) for each individual equalizer channel is done through a 3x3 header. There are four sets of headers, one for each equalizer channel. Figure 5 illustrates the location of the headers.

The notation CP[1-4]_[A,B] refers to the QLx411G series quad equalizer control pins. They are associated with the 4 channels 2-bit number where 'A' is the MSB and 'B' is the LSB. Table 3 describes the relationship between the CPs and the five equalizer boost settings. Bit A is binary (Jumper to Low, No Jumper), while bit B is tri-state (Jumper to Low, No Jumper, Jumper to High).

TABLE 3. CP BOOST SETTINGS

CP[1-4]A	CP[1-4]B	BOOST LEVEL
Jumper to Low	Jumper to Low	0
Jumper to Low	No Jumper	1
Jumper to Low	Jumper to High	2
No Jumper	Jumper to Low	3
No Jumper	No Jumper	4

Schematic and Bill Of Materials

The schematic of the evaluation board is illustrated in Figure 6. The silk screen shots of the top and bottom of the board are shown in Figure 7. The Bill of Materials can be found in Table 4.

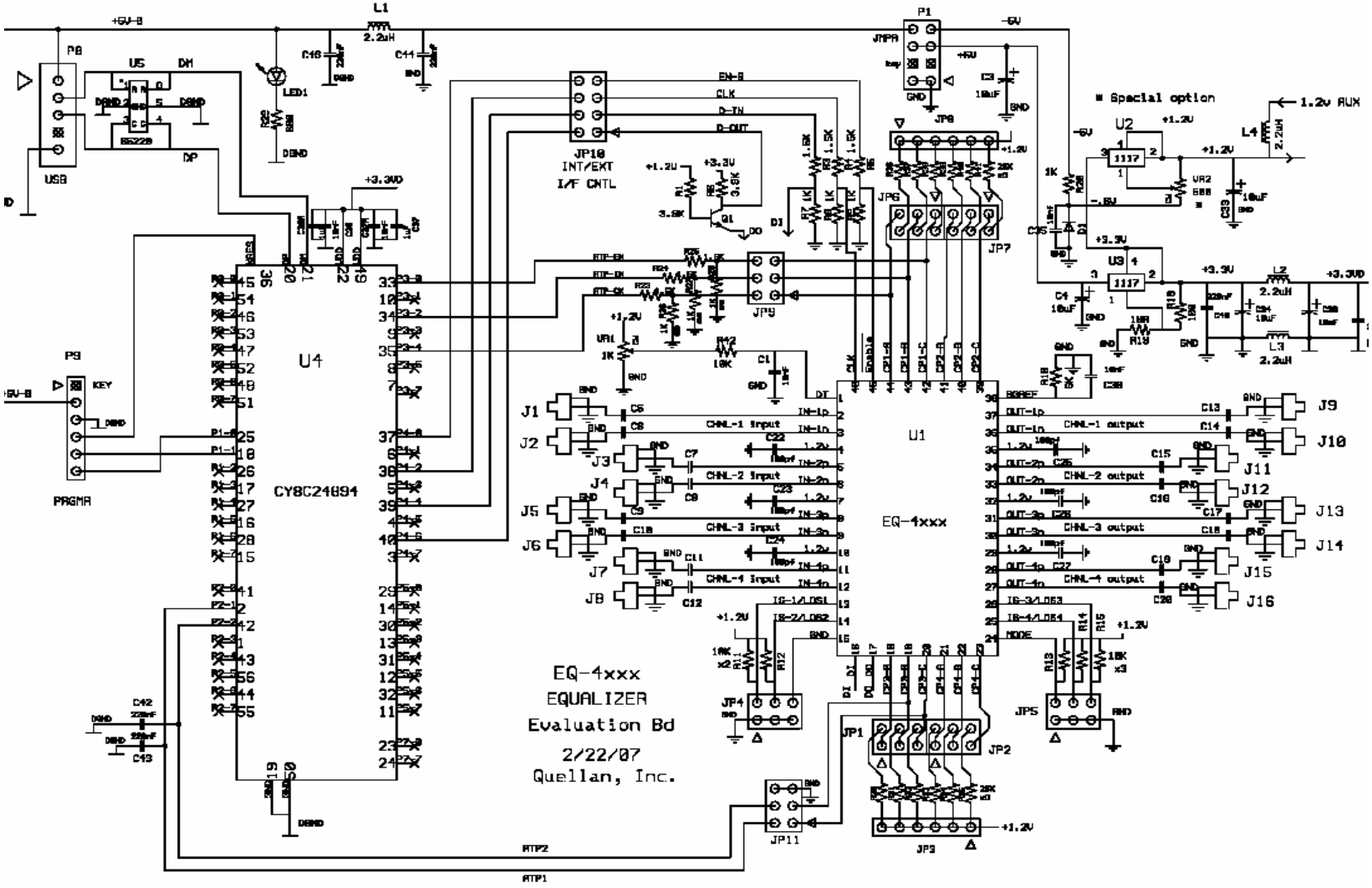

FIGURE 6. SCHEMATICS OF THE QLx411G EVALUATION BOARD

Silk Screens

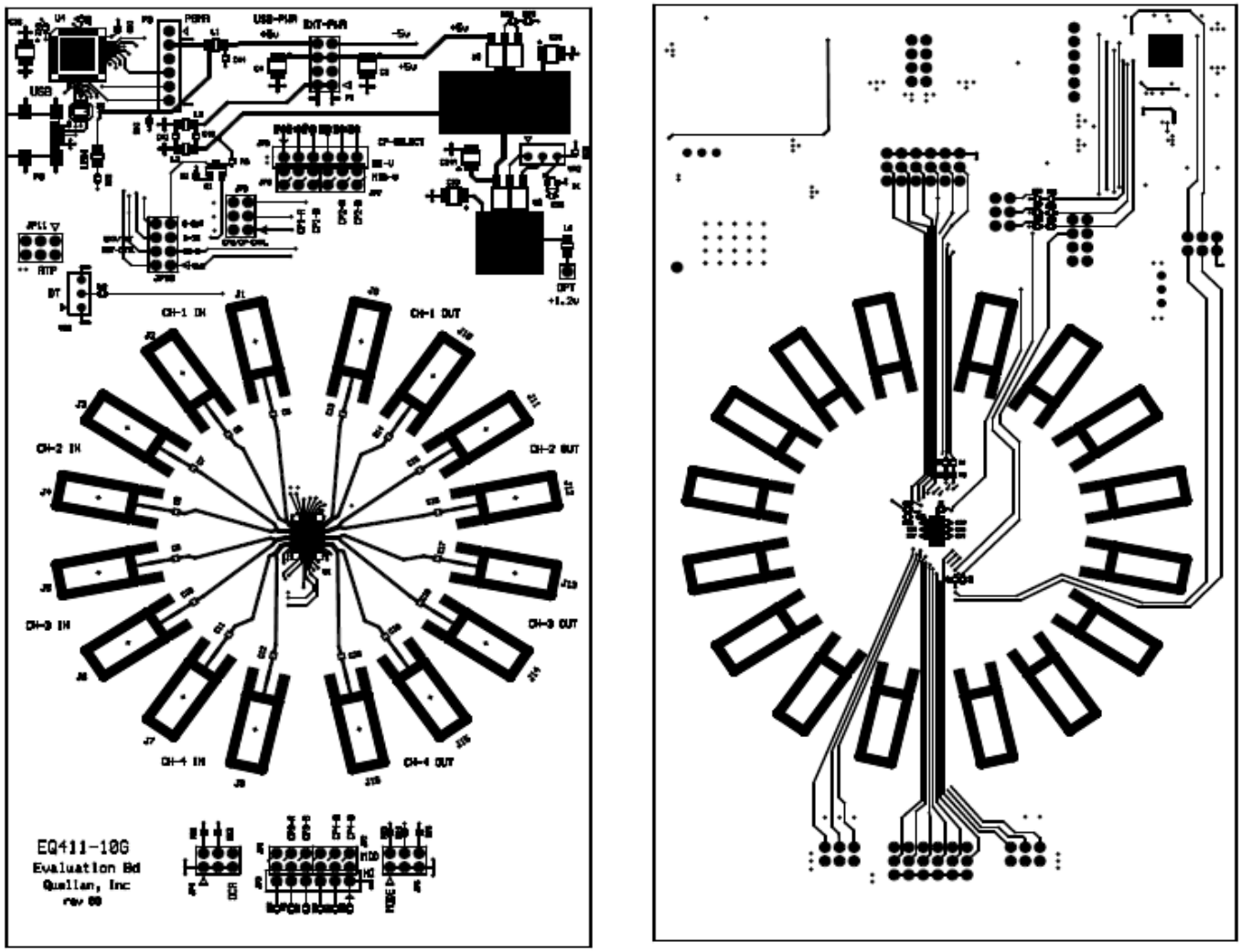

FIGURE 7. QLx411G EVALUATION BOARD TOP (LEFT) AND BOTTOM (RIGHT) SILK SCREENS

TABLE 4. QLx411G EVALUATION BOARD BILL OF MATERIALS

REF DES	TOP/ BOT	DESCRIPTION	PART NO. (DIGIKEY)	QTY	25 BRD QTY	MURATA SUB
TOP SIDE						
C36, C37 Note: On C36, C37 - install 10nF first, then 1µF on top.	T	10nF/1µF double-stack	PCC103BQCT-ND/ PCC2268CT-ND	2/2	50/50	**GRM36C06103K25D500**/ n/a
C3, C4, C33, C34, C34A, C39	T	10µF TANT CAP	478-1673-1-ND	6	150	GRM40X5R106K16H539
C40, C41, C42, C43, C44, C45	T	220nF	PCC2272CT-ND	6	150	GRM36Y5V224Z16D500
C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20	T	220nF wideband	BB0502Y5V224M16NVT98205	16	400	

TABLE 4. QLx411G EVALUATION BOARD BILL OF MATERIALS (Continued)

REF DES	TOP/ BOT	DESCRIPTION	PART NO. (DIGIKEY)	QTY	25 BRD QTY	MURATA SUB
C1A, C2A, C3A, C4A, C5A, C6A, C7A, C8A, C9A, C10A, C11A, C12A, C13A, C14A, C15A, C16A	T	10nf 0402	PCC103BQCT-ND	16	400	GRM36X7R103K25D500
D1	T	0Ω 0603	P0.0GCT-ND	1	25	
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16	T	SMA VERT MNT	A24691-ND	16	400	
JP1, JP2, JP4, JP5, JP6, JP7	T	2x3 HDR	WM26806-ND	6	150	
JP10, P1 Note: cut keying pin on P1 per drawing	T	2x4 HDR	WM26808-ND	2	50	
JP3, JP8, P9 Note: cut keying pin on P9 per drawing	T	1x6	WM6506-ND	3	75	
L1, L2, L3, L4	T	1206 SMD IND	LQH31CN2R2M03L (Murata)	4	100	
LED1	T	1206 LED	350-1566-1-ND	1	25	
P8	T	USB CONN	H2959CT-ND	1	25	
Q1	T	NPN XSISTOR	2SC248000LCT-ND	1	25	
R1, R6	T	3.9k	P3.9KJCT-ND	2	50	
R11, R12, R13, R14, R15, R42	T	10k	311-10.0KLRCT-ND	6	150	
R18	T	100	311-100JRCT-ND	1	25	
R29	T	680Ω	P680JCT-ND	1	25	
R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41	T	25k	541-25.5KLCT-ND	12	300	
R19	T	180	P180JCT-ND	1	25	
U2, U3	T	LM-1117 VOLT REG	LM1117MP-ADJCT-ND	2	50	
U4	T	CY8C24894 MCU	CY8C24894-24LFXI (Cypress)	1	25	
U5	T	65220 ESD	296-9694-1-ND	1	25	
VR1	T	1k TRIM POT	CT94EW102-ND	1	25	PV36W102C01B00
VR2 jumper	T	**Do not install pot.** Wire jumper pin 2 to pin 3	n/a	1	25	PV36W501C01B00 Do not install SM component
BOTTOM SIDE						
C1, C38	B	10nF	PCC103BQCT-ND	2	50	
C22, C23, C24, C25, C26, C27	B	100pF	PCC101CQCT-ND	6	150	GRM36X7R101J25D50
R10	B	6k	P6.04KLCT-ND	1	25	
R3, R4, R5, R23, R24, R25	B	1.5k	P1.5KJCT-ND	6	150	
R7, R8, R9, R26, R27, R28	B	1k	RHM1.00KLCT-ND	6	150	
DO NOT INSTALL						
C35, JP9, JP11, R20, VR2, C22, C23, C24, C25, C26, C27						

About Q:ACTIVE®

Intersil has long realized that to enable the complex server clusters of next generation datacenters, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE® product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency, and cable gauge size as well as increased airflow in tomorrow's datacenters. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding datacenter.

Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow, and improves power consumption.